INTEGRATED CIRCUIT HAVING A DATA PROCESSING UNIT AND A BUFFER MEMORY

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Background of the Invention:

Field of the Invention:

The invention lies in the field of integrated circuits. The invention relates to an integrated circuit having a data

10 processing unit and a buffer memory.

An integrated circuit is conventionally tested by having the integrated circuit be supplied with test data from a tester. The output values obtained depending on the applied test data

15 are transferred back to the tester and checked there. If the tester ascertains that a value transferred back does not correspond to a desired value, a defect is identified.

To repair defects in integrated circuits, provision is often

20 made of setting memories that are written to after the conclusion of a test, e.g., to disconnect defective circuit areas and replace them by redundant circuit elements that are additionally provided on the integrated circuit. Such disconnect is performed by using so-called fuses, which

25 represent switches that are initially closed or open and are then opened or closed, respectively, depending on the setting

to be performed, with the aid of a suitable programming circuit.

The calculation of the required settings is conventionally carried out in an external tester. The procedure is very time-intensive, in particular, due to the data transfer from and to the tester. If it is desired to determine the settings that are to be performed in the tested integrated circuit, then it is necessary to provide an integrated processing circuit including register memories in which the settings are calculated. In the case of memory modules, such a processing circuit would have to optimize the settings that are to be performed by a redundancy calculation, the settings then activating replacement elements for defect addresses in a memory array. The redundancy calculation in the processing unit is usually carried out by an iterative method. Determining corresponding settings in the circuit to be tested has the disadvantage that a considerable additional outlay on circuitry would be necessary for the processing circuit that carries out the redundancy calculation.

Summary of the Invention:

It is accordingly an object of the invention to provide an integrated circuit having a data processing unit and a buffer memory that overcomes the hereinafore-mentioned disadvantages of the heretofore-known devices and methods of this general

type and that makes possible the determination of the

individual settings for the setting memory and minimizes the

required outlay on circuitry.

5   With the foregoing and other objects in view, there is

provided, in accordance with the invention, an integrated

circuit, including a data processing unit, a buffer memory

having registers for storing data for the data processing

unit, and a setting memory connected to the buffer memory.

10   The buffer memory is connected to the data processing unit.

The setting memory can be written to and/or read from through

the buffer memory.

The invention has the advantage that it is possible to perform

15   a redundancy calculation for determining the setting values

for the setting memory in the integrated circuit that is

tested. The requisite circuit, which has a data processing

unit, a buffer memory, and a setting memory, in order to carry

out the required calculations, would have a non-negligible

20   area requirement in the integrated circuit due to the outlay

on circuitry for the register memory. The additional area

requirement can be minimized by virtue of the fact that the

invention provides for the buffer memory already available in

the integrated circuit for writing to the setting memories

25   also to be used as a register for a data processing unit. All

that is necessary is an additional outlay on circuitry for the
processing unit, but not for the register memories.

In accordance with another feature of the invention, the
integrated circuit has circuit elements for replacing
defective circuit areas. The circuit elements can be
activated by the setting memory. Preferably, the circuit
elements are memory elements that replace defective memory
areas of a memory. In such a case, it is particularly
advantageous to perform the determination of the settings in
the integrated circuit to be tested, because, in particular,
the optimal utilization of the available circuit elements that
are intended to replace the defective memory areas can be
calculated only with some computation complexity. The
requisite settings are usually determined iteratively, i.e.,
in a computationally intensive approximation method. With the
apparatus according to the invention, it is possible to carry
out the requisite computation operations in parallel in the
respective integrated circuit, thereby making it possible to
save computation capacity in a tester.

In accordance with a further feature of the invention, the
processing unit has an arithmetic logic unit (ALU). Such an
arithmetic logic unit is usually constructed so that coded
instructions in a program memory are applied to the contents
of one or more registers. Furthermore, the buffer memory of

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the integrated circuit is subdivided into a plurality of

registers, at least one register being provided for the data

to be processed and a further register being provided for

coded instructions for the ALU. In such a case, the

5   integrated circuit preferably has two data registers for the

data to be processed. Such a configuration is advantageous so

that a program register for the coded instructions and two

data registers are provided, with whose contents arithmetic or

logical operations can be executed in accordance with the

10 instructions. The result is written back to one of the data

registers. Because the data can be written to the register

cells through the arithmetic logic unit, it is possible for

the ALU to write the determined settings directly to the

relevant position of the buffer memory for the setting memory.

15 Thus, a considerable amount of time can be saved because the

transfer of determined data from the integrated circuit to the

tester and/or vice versa is obviated.

In accordance with an added feature of the invention, the

20 buffer memory is two buffer memories each containing data to

be processed.

In accordance with an additional feature of the invention, the

buffer memory is a latch.

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In accordance with yet another feature of the invention, the buffer memory has a shift register.

In accordance with yet a further feature of the invention, the

5   shift register has at least one switch subdividing the shift register into registers for the processing unit.

In accordance with yet an added feature of the invention, the processing unit serially writes to and reads from each of the

10   registers.

In accordance with a concomitant feature of the invention, the setting memory has electrical fuses.

15   With the objects of the invention in view, there is also provided a method for determining setting data for a setting memory from address data, stored in a register, of memory areas of a memory that have been identified as defective depending on instruction data stored in a register, including

20   the steps of providing an integrated circuit having a data processing unit, a buffer memory having register, and a setting memory, storing data for the data processing unit in registers of the buffer memory, connecting the buffer memory to the data processing unit, connecting the setting memory to

25   the buffer memory, and writing to and/or reading from the setting memory through the buffer memory.

Other features that are considered as characteristic for the
invention are set forth in the appended claims.

5   Although the invention is illustrated and described herein as
embodied in an integrated circuit having a data processing
unit and a buffer memory, it is, nevertheless, not intended to
be limited to the details shown because various modifications
and structural changes may be made therein without departing
10   from the spirit of the invention and within the scope and
range of equivalents of the claims.

The construction and method of operation of the invention,
however, together with additional objects and advantages
15   thereof, will be best understood from the following
description of specific embodiments when read in connection
with the accompanying drawings.

Brief Description of the Drawing:

20   The figure is a block circuit diagram of an integrated circuit
according to the invention.

Description of the Preferred Embodiments:

Referring now to the figure of the drawings in detail there is
25   shown block circuit diagram of an integrated circuit in
accordance with a preferred embodiment of the invention. A

setting memory 1 with setting memory cells 2 is situated in a

non-illustrated integrated circuit. The setting memory 1

serves for activating redundant circuit areas, in particular,

redundant memory areas, in order, thereby, to replace

5   defective areas of a non-illustrated memory array. The

setting memory 1 is connected to a latch 3 with latch cells 4

so that each setting memory cell 2 is associated with a latch

cell 4. The latch 3 is subdivided into a first latch area 5,

a second latch area 6, and a third latch area 7. The latch

10   cells 4 in each of the latch areas 5, 6, 7 are connected up as

shift registers, i.e., the output of one latch cell is

connected to the input of a next latch cell 4. The first

latch area 5 and the second latch area 6 preferably have the

same number of latch cells 4 in each case. However, it may

15   also be provided that the number of latch cells 4 in the first

latch area 5 differs from that in the second latch area 6.

The respective first and last latch cells of the latch cells 4

of the three latch areas 5, 6, 7 are provided with the

20   reference symbols 41, 43, 45 and 42, 44, 46, respectively.

The output of the last latch cell 42 of the first latch area 5

is switchably connected through a switch S1 to the input of

the first latch cell 43 of the second latch area 6, so that a

shift register including the first and second latch areas is

25   formed when the switch is closed. Equally, the output of the

last latch cell 44 of the second latch area 6 is switchably

connected through a switch S2 to an input of the first latch

cell 45 of the third latch area 7, so that a shift register is

formed by the second latch area 6 and the third latch area 7

when the switch S2 is closed. If both switches S1 and S2 are

5   closed, all the latch cells 4 together form a shift register.

The outputs of the last latch cells 42, 44 of the first latch

area 5 and of the second latch area 6 are connected

respectively to a processing unit 8, so that the data in the

10   latch areas 5, 6, 7 can be read serially. An output of the

processing unit 8 is connected to an input of the first latch

cell 41 of the first area 5. The output of the last latch

cell 46 of the third latch area 7 is connected, on one hand,

to an input of the processing unit 8 and is switchably

15   connected, on the other hand, through a switch S3 to the input

of the first latch cell 45 of the third latch area 7. The

switches S1, S2, and S3 are controlled through the processing

unit 8. Furthermore, a non-illustrated external tester is

connected to the input of the first latch cell 41 of the first

20   area 5, through which tester the latch cells can be written to

or read from.

To generate setting data for the setting memory 1 from defect

data, i.e., defective output data given the presence of a

25   specific test pattern, such as, e.g., addresses of defective

memory cells, the defect data must usually be processed in an

algorithm. The result of the algorithm then constitutes

setting data that are stored in the setting memory 1. In

conventional test systems, the calculation is carried out in a

non-illustrated external tester, i.e., the defect data are

5   transferred to the external tester, where the calculation is

carried out, and then the setting data are transferred back

into the integrated circuit for storage in the setting memory

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10   In the exemplary embodiment according to the invention, the

integrated circuit is provided in a memory module. After

being written to, the setting memory 1 then receives setting

values, whereby redundancy memory areas are enabled that

replace defective memory cells in a main cell array. Because

15   both word and bit lines and individual cells can be replaced

by the setting memory, it is expedient to combine, in an

algorithm, defective cells, if possible, to form word or bit

lines that are then replaced by a redundant word or bit line

provided therefor.

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The integrated circuit according to the invention makes it

possible to carry out the calculation in the memory module.

As a result of using the latch cells 4 for the setting memory

cells 2 as registers for the processing unit 8, a considerable

25   amount of area can be saved on the memory module.

A redundancy calculation is carried out as set forth below.

First, the determined defect data and the processing instructions are made available by the non-illustrated tester

5 and are then written serially to the latch 3, constructed as a shift register, so that the first latch area 5 and the second latch area 6 contain defect data and the third latch area 7 contains instruction data. To write such data to the latch 3, the switches S1 and S2 must be closed, so that the entire

10 latch 3 forms a uniform shift register. However, data that are generated in the integrated circuit or are stored there can also be written to the latch 3. Thus, by way of example, data from a desired/actual comparison that takes place in the integrated circuit can be written to the latch areas 5, 6 and

15 program data from a ROM memory can be written to the latch area 7.

If the latch 3 contains the data provided, the processing unit 8 begins to execute the instruction in the third latch area 7.

20 To that end, the switches S1 and S2 are opened and switch S3, depending on whether or not cyclic processing is necessary, is closed. The content of the last latch cell 46 of the third area 7 is then read out by being shifted toward the right into the processing unit 8. In such a case, the content of the

25 last latch cell 46 is written to the first latch cell 45 of the third latch area 7 again if the switch S3 is closed.

In accordance with the received instruction, the processing
unit 8 reads in the content of the last latch cell 42 of the
first latch area 5 and/or the content of the last latch cell

5   44 of the second latch area 6 and combines these contents in
accordance with the received instructions. The result is
written to the first latch cell 41 of the first latch area 5,
and all of the positions of the latch cells 4 are shifted
toward the right, the content of the last latch cell 42 of the

10   first latch area being read into the processing unit 8.

The processing cycle is repeated a predetermined number of
times and, in the process, successively through a shifting-
toward-the-right of the latch cells of the first area 5 and/or

15   of the latch cells 4 of the second latch area 6, all the latch
cells of the first latch area 5 and of the second latch area 6
are processed in accordance with the received instruction in
the processing unit 8. With the read-out of the contents of
the latch cells 4 of the first latch area 5, the respective

20   result of the processing is simultaneously written to the
first latch area 5 at the input of the first latch cell 41 of
the first latch area 5.

After the specific number of cycles has taken place, the

25   instruction has been processed and the next instruction is
read from the last latch cell 46 of the third latch area 7

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into the processing unit 8 by a shifting-toward-the-right

process. In the processing unit 8, as described above, the

content of the latch cells 4 of the first latch area 5 and/or

the content of the latch cells of the second latch area 6

5   are/is processed in accordance with the instruction and the

result is written in each case to the first latch cell 41 of

the first latch area 5. The processes of read-out and writing

to the latch area 5 and the second latch area 6 are effected

by the contents being shifted toward the right.

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The processing unit 8 can likewise provide, through control of

the switch S1, for the contents of the first latch area 5 to

be transferred into the second latch area 6 by a shifting-

toward-the-right process. Analogously, it is also possible to

15   transfer contents of the second latch area 6 through the

processing unit 8 - controlled by instructions stored in the

third latch area 7 - into the first latch area 5.

Furthermore, it is possible, by the closing of the switch S2

and opening of the switch S3, to transfer the content of the

20   second latch area 6 into the third latch area 7. As such, it

is also possible to load a result of a previously effected

operation into the third latch area 7, the instruction memory,

which means that it is possible to carry out complex program

sequences that depend on the result of previous operations.

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Furthermore, it is possible for the integrated circuit

according to the invention to use only some of the available

latch cells 4 as register cells. By way of example, the

output of the last latch cell 46 of the third area 7 could be

5   connected through a further non-illustrated switch to further

latch cells 4 associated with respective setting memory cells

2. As a result, it would be possible to store setting values

already determined for the setting memory 1 in the relevant

latch cells 4 without these values having to be transferred

10   beforehand to the external tester for buffer-storage or the

like.

It goes without saying that the latch cells 4 can also be

subdivided into more than three areas. This means that it is

15   possible to perform even more complex operations with more

than two registers in the processing unit 8.

The closing of the switch S3 effects feedback of the program

memory in the third latch area 7, so that a predetermined

20   sequence of instructions can be executed repeatedly. Such a

process is preferably suitable for carrying out iterative

calculation methods that have to be performed, in particular

in the optimization of setting values from defect data. The

optimization enables a considerable amount of computation time

25   to be saved, because, during a test run, the integrated

modules can carry out in parallel computation operations that

would have taken place in the tester according to a
conventional method.

The size of the latch areas 5, 6, 7 can be chosen arbitrarily.

5   It is expedient, however, to provide the first and second
latch areas 5, 6 in the size of a memory address to be able to
process addresses of defective memory cells and to provide the
third latch area 7 in a size sufficient for the operations for
the processing unit 8.

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The features of the invention that are disclosed in the above
description, the drawing and the claims may be of importance
both individually and in any desired combination for the
realization of the invention in its various configurations.